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06EC46

Fourth Semester B.E. Degree Examination, June/July 2016
Linear IC's and Applications

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer FIVE full questions, selecting at least TWO questions from each part.***
2. ***Missing data if any may be suitably assumed.***

PART – A

1 a. Explain the following terms with reference to OPAMP:
i) Input off-set voltage
ii) Input bias current
iii) Slew rate **(12 Marks)**

b. Design a noninverting amplifier circuit shown in Fig.Q1(b) to meet the following specifications. Use 741 OPAMP voltage gain = 50, signal amplitude = 10 mV. I_{Bmax} for 741 OPAMP = 500 nA. (From data sheet)

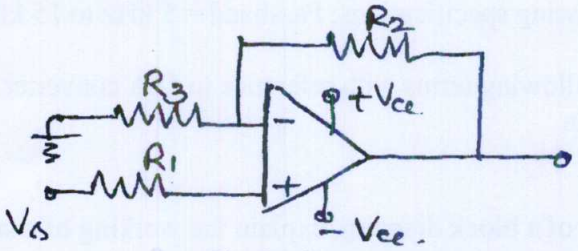

Fig.Q1(b) **(08 Marks)**

2 a. Briefly discuss the upper cutoff frequency of an OPAMP circuit and show, how the cutoff frequency can be set for inverting, non-inverting and difference amplifier. **(12 Marks)**

b. A capacitor coupled voltage follower is to be designed to have a lower cutoff frequency of 120 Hz. The load resistance is 8.2 KΩ and the OPAMP used has a maximum input bias current of 600 nA. Design a suitable circuit. **(08 Marks)**

3 a. Show now the slew rate of an OPAMP can produce distortion in a sinusoidal output waveform. Also, explain how the slew rate can limit the amplitude of the distortion free sinewave output for a given OPAMP cutoff frequency. **(12 Marks)**

b. i) Calculate the cutoff frequency limited rise time for a voltage follower circuit using a 741 OPAMP. Also determine the slew rate limited rise time if the output amplitude is to be 5V and cutoff frequency f_2 = 800 KHz.
ii) Determine the max undistorted pulse output amplitude for the 741 voltage follower, if the output rise time is not to exceed 1 μsec.
iii) Calculate the min rise time and the max pulse amplitude at that rise time for a 741 amplifier with an upper cutoff frequency of 100 kHz. **(08 Marks)**

4 a. Sketch the complete circuit of an instrumentation amplifier. Discuss the characteristics of the circuit and show how the voltage gain can be varied. **(10 Marks)**

b. With a neat diagram, explain the working of a sample and hold circuit. Discuss the hold time and acquisition time. **(10 Marks)**

PART – B

5 a. With the help of a neat circuit diagram, explain the working of a fullwave precision rectifier circuit. Mention its advantage. **(12 Marks)**

b. Design a RC phase shift oscillation using 741 IC chip. For an oscillating frequency of 2 kHz. The supply voltage = ±15V. **(08 Marks)**

6 a. With a neat circuit diagram and relevant waveforms (at pin no 2, 3 and 6 of 741 OPAMP), explain the working of a monostable multivibrator circuit using OPAMP. **(12 Marks)**

b. An Astable multi-vibrator using 555 timer is connected with R_a = 2.2 KΩ, R_b = 6.8 KΩ, c = 0.1 μf, calculate:

i) t_{high}
ii) t_{low}
iii) free running frequency
iv) duty cycle. **(08 Marks)**

7 a. Write notes on:

i) Phase loured loop
ii) 723 regulator **(12 Marks)**

b. Design a bandwidth filter (Bpf) with the suitable contribution of Lpf and Hpf (1^{st} order) to meet the following specifications: Passband = 5 kHz to 15 kHz. **(08 Marks)**

8 a. Explain the following terms with reference to D/A converter:

i) Resolution
ii) Accuracy
iii) Linearity **(10 Marks)**

b. With the help of a block diagram, explain the working of a successive approximation type of A/D converter. **(10 Marks)**

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